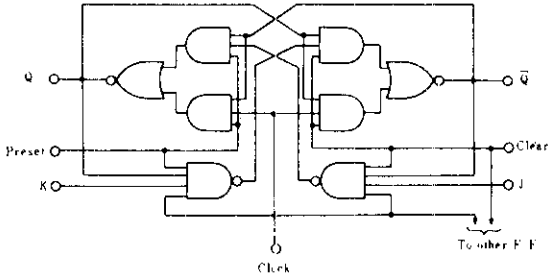
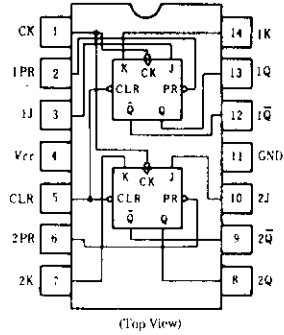


HD74LS78A ● Dual J-K Flip-Flops (with Preset, Common Clear, and Common Clock)

■ BLOCK DIAGRAM (1/2)



■ PIN ARRANGEMENT

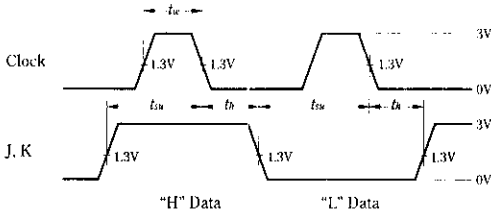


■ RECOMMENDED OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Clock frequency	f_{clock}	0	—	30	MHz
Pulse width	Clock High	20	—	—	ns
	Preset Clear Low	t_w	25	—	—
Setup time	"H" Data	$20\downarrow$	—	—	ns
	"L" Data	$20\uparrow$	—	—	ns
Hold time	t_h	$0\downarrow$	—	—	ns

Note) \downarrow : The arrow indicates the falling edge.

■ TIMING METHOD



■ FUNCTION TABLE

Inputs					Outputs	
Preset	Clear	Clock	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q ₀	Q̄ ₀
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	X	X	Q ₀	Q̄ ₀

Notes) H; high level, L; low level, X; irrelevant

\downarrow ; transition from high to low level

Q₀; level of Q before the indicated steady-state input conditions were established.

Q̄₀; complement of Q₀ or level of Q̄ before the indicated steady-state input conditions were established.

Toggle; each output changes to the complement of its previous level on each active transition indicated by \downarrow .

*; This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

■ ELECTRICAL CHARACTERISTICS (Ta = -20 ~ +75°C)

Item	Symbol	Test Conditions	min	typ*	max	Unit	
Input voltage	V _{IH}		2.0	—	—	V	
	V _{IL}		—	—	0.8	V	
Output voltage	V _{OH}	V _{CC} = 4.75V, V _{IH} = 2.7V, V _{IL} = 0.8V, I _{OH} = -400μA	2.7	—	—	V	
	V _{OL}	V _{CC} = 4.75V, V _{IH} = 2V, I _{OL} = 8mA	—	—	0.5	V	
		V _{IL} = 0.8V, I _{OL} = 4mA	—	—	0.4		
Input current	J, K	V _{CC} = 5.25V, V _I = 2.7V	—	—	20	μA	
	Clear		—	—	120		
	Preset		—	—	60		
	Clock		—	—	160	mA	
	J, K		V _{CC} = 5.25V, V _I = 0.4V	—	—		-0.4
	Clear			—	—		-1.6
Preset	—	—		-0.8			
Clock	—	—	-1.6	mA			
J, K	V _{CC} = 5.25V, V _I = 7V	—	—		0.1		
Clear		—	—		0.6		
Preset		—	—		0.3		
Clock		—	—	0.8			
Short circuit output current	I _{OS}	V _{CC} = 5.25V	-20	—	-100	mA	
Supply current ***	I _{CC}	V _{CC} = 5.25V	—	4	6	mA	
Input clamp voltage	V _{IK}	V _{CC} = 4.75V, I _{IN} = -18mA	—	—	-1.5	V	

* V_{CC} = 5V, Ta = 25°C

** I_{IL} should not be measured when preset and clear inputs are low at same time.

*** With all outputs open, I_{CC} is measured with the Q and Q̄ outputs high in turn.

At the time of measurement, the clock input is grounded.

HD74LS78A

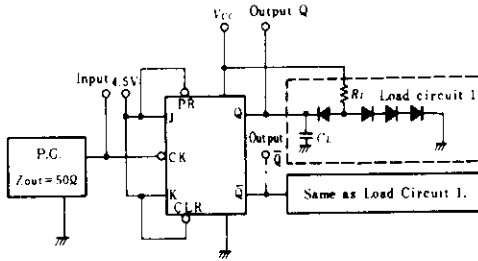
SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $T_a=25^\circ C$)

Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}			$C_L = 15pF$, $R_L = 2k\Omega$	30	45	-	MHz
Propagation delay time	t_{PLH}	Clear Preset Clock	Q, \bar{Q}		-	15	20	ns
	t_{PHL}				-	15	20	ns

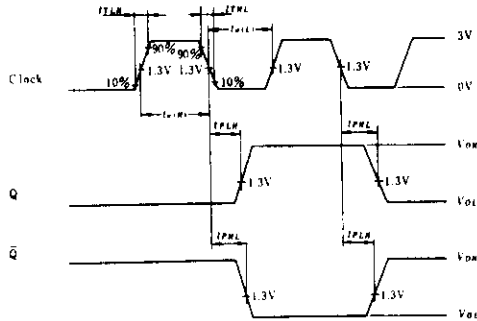
TESTING METHOD

1) Test Circuit

1.1) f_{max} , t_{PLH} , t_{PHL} (Clock \rightarrow Q, \bar{Q})

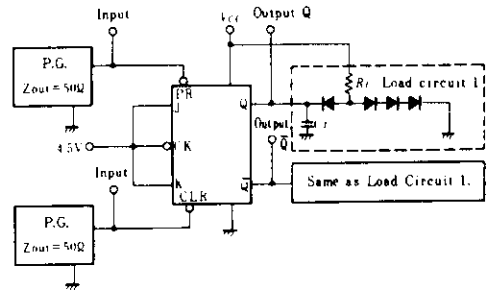


- Notes) 1. Test is put into the each flip-flop
 2. All diodes are 1S2074 \oplus .
 3. C_L includes probe and jig capacitance.

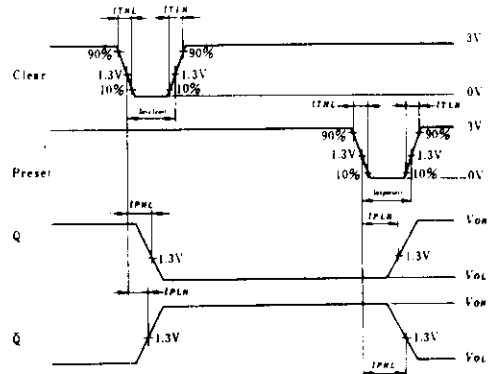


Note) Clock input pulse: $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$,
 $PRR=1MHz$, duty cycle=50% and: for f_{max} ,
 $t_{TLH}=t_{THL} \leq 2.5ns$.

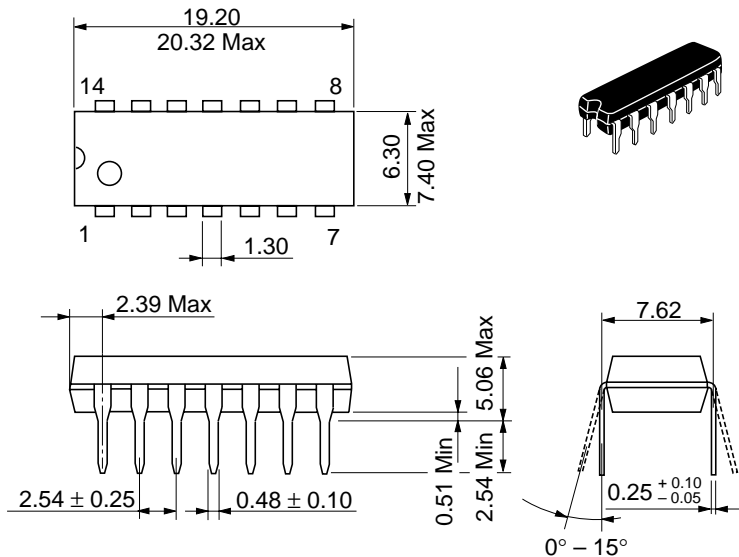
1.2) t_{PHL} , t_{PLH} (Clear, Preset \rightarrow Q, \bar{Q})



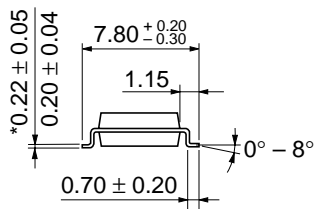
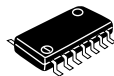
- Notes) 1. Test is put into the each flip-flop
 2. All diodes are 1S2074 \oplus .
 3. C_L includes probe and jig capacitance.



Note) Clear and preset input pulse: $t_{TLH} \leq 15ns$,
 $t_{THL} \leq 6ns$, $PRR=1MHz$



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EIAJ	Conforms
Weight (reference value)	0.97 g



Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
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